Amendments to the Claims:

This listing of claims will replace all prior versions, and listings, of claims in the application:

Listing of Claims:

1-19. (Canceled).

20. (Currently Amended) A reconfigurable device for data processing via a ~~dynamical runtime reconfiguration~~ method of reconfiguration during runtime, comprising:

a plurality of processing array elements that are reconfigurable at a runtime by ~~reconfiguration~~ configuration information;

a plurality of configurable data busses adapted to transmit data in a multi-dimensional way, at least some of the plurality of processing array elements configurable for connection to said busses to provide non-next-neighbor connections, wherein said at least some processing array elements include ~~coarse grained~~ units for arithmetic and logic operations, at least one of the ~~coarse grained~~ units including:

a stage for arithmetic operations, the stage including a multiplier stage and an adder stage;

at least one input and at least one output for data;

a first plurality of registers;

a return path; and

at least one multiplexer;

an element for configuring and reconfiguring ~~a program load unit~~; and

an interconnection selection element [[unit]] adapted to selectively interconnect said at least one of the ~~coarse grained~~ units with others of the ~~coarse grained~~ units;

wherein:

a first subset of said first plurality of registers is provided for said at least one input and at least one output and allows for decoupling of at least one of said at least one input and said at least one output from said busses by storing of operand inputs;

said multiplier stage is connectable to: (a) at least two input registers of said first subset for receiving an input of two operands; and (b) said adder stage, said connections to (a) and (b) being such that a selection can be made between at least two of:

(i) adding the two operand inputs;

(ii) adding an output of said multiplier stage and a further operand input;

(iii) the output of said multiplier stage and results of the at least one ~~coarse grained~~ unit; and

(iv) one of the [[an]] operand inputs [[input]] and an output of a result of the at least one ~~coarse grained~~ unit;

said return path is adapted to return a result of said at least one ~~coarse grained~~ unit from an output register of said first subset as an operand via said at least one multiplexer for selecting for further processing one of an external operand input and a result;

said at least one multiplexer is arranged between an input register of said first subset and said adder stage so as to allow said at least one ~~coarse grained~~ unit to selectively have direct access to its own results which are returned as operands for calculations in a serial manner;

said at least one adder stage is bypassable by allowing for an addition of a zero as one operand input;

said plurality of processing array elements are partially ~~dynamically~~ reconfigurable at run time in their function; and

the function and [[an]] interconnection of said plurality of processing array elements are programmed in components [[units]] specifically accessible by ~~a program load unit~~ the element for configuring and reconfiguring.

21. (Currently Amended) The reconfigurable device of claim 20, wherein said plurality of processing array elements are partially ~~dynamically~~ reconfigurable at run time in their interconnection.

22. (Previously Presented) The reconfigurable device of claim 21, wherein at least some registers of the reconfigurable device are shift registers that provide shift capabilities.

23. (Previously Presented) The reconfigurable device of claim 22, wherein said plurality of processing array elements includes at least one array element having an arithmetic and logic unit, a bus access from a data processing in said arithmetic and logic unit being decoupled via registers so that said at least one array element is independently functional.

24. (Currently Amended) The reconfigurable device of claim 23, further comprising:

a second plurality of registers which communicate with the at least one ~~coarse grained~~ unit for storing data relating to a configurable function of the at least one ~~coarse grained~~ unit and data relating to an interconnection of stages within the at least one ~~coarse grained~~ unit.

25. (Currently Amended) The reconfigurable device of claim 24, wherein said element for configuring and reconfiguring ~~program load unit~~ is configured for:

accessing specific registers of said second plurality of registers for at least one of:

storing the data relating to the configurable function;

selectively transferring to said specific registers the data relating to the configurable function; and

selectively transferring to said specific registers the data relating to the configurable interconnection.

26. (Currently Amended) The reconfigurable device of claim 25, wherein the data relating to the configurable function of and the interconnection of stages within the at least one ~~coarse grained~~ unit forms a configuration vector that is set through a function control interface and refers to a number of possible instructions, said possible instructions being such that, for any one of the number of possible instructions, a response of any one of the at least some of the plurality of processing array elements to said data that refers to the number of possible instructions is identical to a response of any other of the at least some of the plurality of processing array elements to said number of possible instructions, said responses remaining the same over time such that transmitted ones of the number of possible instructions statically correspond to a constant one of possible operations.

27. (Currently Amended) The reconfigurable device of claim 20, wherein the components [[units]] specifically accessible by the element for configuring and reconfiguring ~~program load unit~~ are registers.

28. (Previously Presented) The reconfigurable device of claim 27, wherein the reconfigurable device is adapted for reconfiguring said plurality of processing array elements in their function and interconnection at run time such that data processing by at least some of said plurality of processing array elements is not inhibited while data relating to a configurable function of and an interconnection of stages within another of said plurality of processing array elements is transferred to ones of the specifically accessible registers.

29. (Previously Presented) The reconfigurable device of claim 28, wherein a register decoupling from a bus of said other processing array elements when said another processing array element is reconfigured by the reconfiguration information at runtime allows the reconfiguration of said another processing element without an interfering effect on data transmitters and receivers in the at least some of said plurality of processing array elements, such that: said plurality of processing array elements are partially reconfigurable; and the at least some of said plurality of processing array elements are able to continue their data processing during the partial reconfiguration.

30. (New) The reconfigurable device of claim 20, wherein said at least some processing array elements are implemented in a Field Programmable Gate array (FPGA).

31. (New) The reconfigurable device of claim 20, wherein said at least some processing array elements output, as a status signal, at least one of a carry-over signal, a A<B signal, and a zero signal, wherein A and B are the two operand inputs.

32. (New) The reconfigurable device of claim 20, further comprising:

a plurality of configuration registers storing configuration information; and

a configuration multiplexer, wherein at least one of the configuration registers is selected via the configuration multiplexer for a reconfiguration of the plurality of processing array elements at runtime.

33. (New) The reconfigurable device of claim 32, further comprising:

a selection device that outputs selection data that controls a selector setting of the configuration multiplexer, wherein which of the configuration registers is selected depends upon the selector setting.

34. (New) The reconfigurable device of claim 33, wherein the selection device is a counter.

35. (New) The reconfigurable device of claim 33, wherein the selection device traverses through a data sequence, the selection data that is output by the selection device depending upon a current point within the traversal.

36. (New) The reconfigurable device of claim 33, wherein the configuration registers are associated with respective bits, each bit indicating a respective subsequent configuration to be loaded, the selection device outputting the selection data according to the bits.

37. (New) The reconfigurable device of claim 33, wherein the configuration registers are associated with respective flags, each flag indicating a respective subsequent configuration to be loaded, the selection device outputting the selection data according to the flags.